

Development of parallel processing algorithms for high-performance computing, maximization of performance of parallel processing systems

»» Hiroki HONDA Laboratory



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Summary of Research

Developing Parallel Processing Technologies for High-Performance Computing

Based on the goal of enhancing processing speeds, an approach involving parallel processing on systems comprised of multiple processors is entering widespread use.

Taking advantage of the growing throughput of computer networks, efforts are also focusing on parallel processing configurations that treat groups of computers on a network as a single multiprocessor system.

To maximize the transparency and convenience of high-performance parallel computing, the process must minimize the tasks performed that the users themselves must perform. This can be done by developing technologies that automate various aspects of the parallel processing environment.

In light of these developments, our laboratory is working to develop parallel processing techniques and end-user assisting technologies to maximize the benefits and performance of high-performance computing systems.

Constraints imposed by power consumption issues have resulted in a leveling off of the performance of a single CPU, prompting a shift in research toward GPUs (Graphics Processing Units) and multicore processors that offer higher performance per unit of power consumed.

However, the processor- and programming method-specific fine tuning required for typical parallel processing configurations pose various difficulties.

To overcome these difficulties, our laboratory is developing a programming framework that will facilitate the tuning process by deploying processors collectively in a more uniform way.

Developing End-User Assisting Technologies

Another research area in which we are devoting considerable effort involves technologies that support end users. The goal of these technologies is to take full advantage of the performance made possible by high-performance computing systems.

In general, the latent performance offered by high-performance computing systems cannot be fully realized at this time unless the users have advanced skills and are capable of performing complicated tuning procedures. This impedes the widespread introduction of these computing systems and calls for technologies that can assist and guide end users.

Developing Grid Construction Technologies

We are also developing grid middleware technologies. The component technologies required to configure a grid include cooperative problem-solving technologies, resource sharing technologies for geographically dispersed environments, and construction and management technologies for virtual composite organizations.

We already offer a library of previously developed automated remote installation and dynamic switching technologies of servers. These should prove essential in reducing time-consuming tasks on the user side.

We are also investigating low power processor architectures, as well as macro data flow processing to overcome the limitations of conventional parallel processing.

Keywords

High-performance computing, GPU computing, GPGPU, grid computing, parallel processing compiler, end-user assisting technology

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Advantages

CREST Project within JST Strategic Basic Research Programs

Within the scope of the JST Strategic Basic Research Programs (CREST Project; 2007-2012) in which we participate, we have completed and presented a proposal to develop a ULP-HPC (Ultra Low Power HPC) capable of achieving a 1000-fold enhancement in performance per unit of power consumption by 2017.

As part of this project, we are developing a unifying programming framework that will make it possible to tune power consumption and performance parameters for GPUs, ClearSpeed FPGA accelerators, and cell processors.

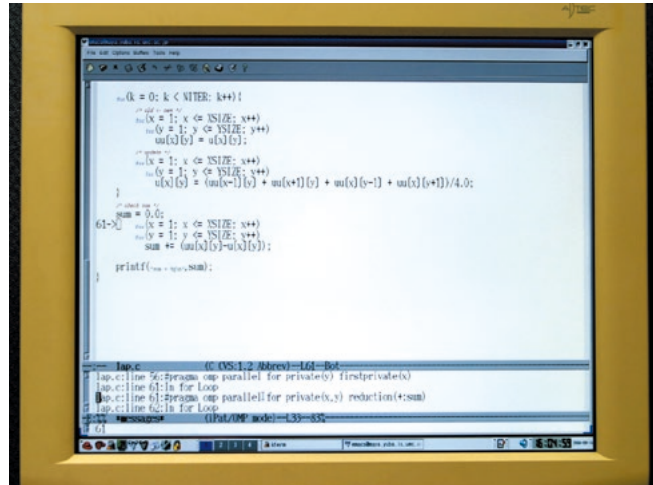
Encompassing a Broad Range of Research Fields Associated with High-Performance Computing

The core theme of the research at our laboratory is high-performance computing. Specific research topics span the spectrum, ranging from processor architecture to system architecture and from system software to applications. This range of interests makes it possible for us to pursue R&D with a bird's-eye view of the broad landscape, unconfined to technologies that are ultimately components of the whole.

Future Prospects

Building a High-Performance Computing System that Organically Integrates Various Approaches to Parallel Processing

To build a high-performance computing substrate, one must exploit the strengths of parallelism intrinsic in applications while achieving a balance with power consumption, and then implement parallel processing on tiers ranging from chip to geographically dispersed environments (e.g., the grid). One of our future goals involves building a high-performance computing system that organically integrates the parallel processing methods developed in each of our studies at an application level.



Parallel processing tool iPat/OMP



Environment for GPGPU experiments



Evaluation environment for many-core processor